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(71) Applicants: SYMETRIX CORPORATION [US/US]; Suite 100, 5055 Mark Dabling Boulevard, Colorado Springs, CO 80918 (US). MATSUSHITA ELECTRONICS CORPORATION [JP/JP]; Takatsuki Osaka, Osaka 569 (JP).

(72) Inventors: AZUMA, Masamichi; Apartment D301, 4820 Nightingale Drive, Colorado Springs, CO 80918 (US). PAZ DE ARAUJO, Carlos, A.; 317 W. Sunbird Cliffs Lane, Colorado Springs, CO 80919 (US). SCOTT, Michael, C.; 4730 Nightingale Drive, #K305, Colorado Springs, CO 80918 (US). UEDA, Toshiyuki; 1340-4, Hokkeji-Higashi-machi, Nara-City, Nara 630 (JP).

(74) Agents: FOREST, Carl, A. et al.; Duft, Graziano & Forest, P.C., Suite 140, 1790 30th Street, Boulder, CO 80301-1018 (US).

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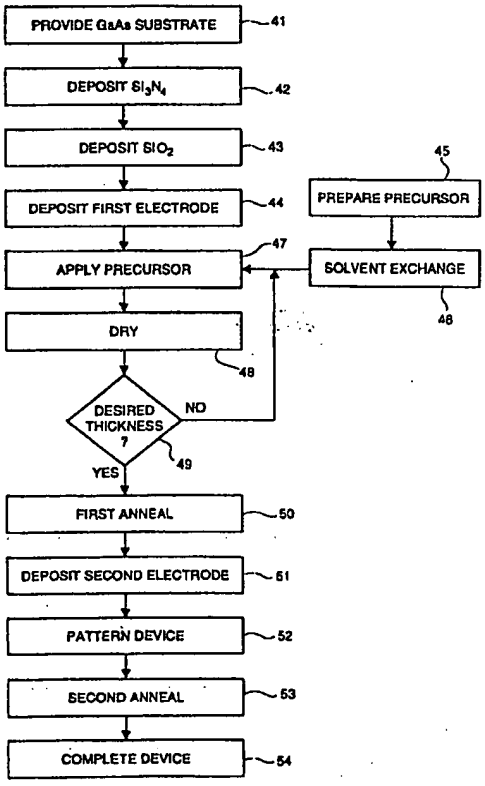
(54) Title: THIN FILM CAPACITORS ON GALLIUM ARSENIDE SUBSTRATE AND PROCESS FOR MAKING THE SAME

(57) Abstract

A silicone nitride barrier layer (12) is deposited on a gallium arsenide substrate (11) to prevent evaporation of the substrate in subsequent heating steps. A silicon dioxide stress reduction layer (14) is deposited on the barrier layer. A first electrode (16) comprising an adhesion layer (18) and a second layer (20) is formed on the stress reduction layer. An essentially anhydrous alkoxycarboxylate liquid precursor is prepared, just before use a solvent exchange step is performed, then the precursor is spun on the first electrode, dried at 400 °C, and annealed at between 600 °C and 850 °C to form a BST capacitor dielectric (22). A second electrode (24) is deposited on the dielectric and annealed.



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THIN FILM CAPACITORS ON GALLIUM ARSENIDE SUBSTRATE AND PROCESS FOR MAKING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention in general relates to the fabrication of integrated circuits utilizing metal oxides, such as barium strontium titanate, and more particularly to the fabrication of thin film capacitors on gallium arsenide substrates.

2. Statement of the Problem

Metal oxide materials, such as barium strontium titanate, commonly referred to as BST, are known to be useful in making integrated circuit thin film capacitors having high dielectric constants. See for example, Kuniaki Koyama, et al., "A Stacked Capacitor With $(Ba_xSr_{1-x})TiO_3$ For 256M DRAM" in *IEDM* (International Electron Devices Meeting) *Technical Digest*, December 1991, pp. 32.1.1 - 32.1.4, and United States Patent No. 5,122,923 issued to Shogo Matsubara et al. In both of these references, the BST capacitors are fabricated on a silicon substrate. While the results were good at low frequencies, i.e., about 10 megahertz, up to now, metal oxide thin film capacitors having high capacitance at high frequencies, i.e., at frequencies of 1 gigahertz and higher, have not been possible.

It has been shown that a PZT ferroelectric RAM can be fabricated on gallium arsenide substrate, and further that silicon nitride (SiN) is effective in encapsulating the GaAs to prevent contamination of the PZT. See "Process Technology Developments For GaAs Ferroelectric Nonvolatile Memory" by L.E. Sanchez et al., and "Integrated Ferroelectrics" by J.F. Scott et al., in *Condensed Matter News*, Vol. 1, No.3, 1992. This article also discloses the use of a silicon dioxide (SiO_2) layer between the silicon nitride and the PZT capacitor. However, while the article indicates that a successful memory was made using the process, it also suggests that, due to problems relating to the interaction of the ferroelectric material with the GaAs, one can expect the electronic properties to be at best the same, but, more likely, less than those of a comparable device built on a silicon substrate.

It is well-known, the process of spin coating has been used for making certain types of insulators in integrated circuits, such as spin-on glass (SOG). A carboxylate-based spin-on process has also been used for making metal oxides such as barium titanate, strontium titanate, and barium strontium titanate. See G.M. Vest and S.Singaram, "Synthesis of Metallo-organic Compounds For MOD Powders and Films", *Materials Research Society Symposium Proceedings*, Vol. 60, 1986, pp.

35-42, Robert W. Vest and Jiejie Xu, "$PbTiO_3$ Thin Films From Metalloorganic Precursors", *IEEE Transactions On Ultrasonics, Ferroelectrics, and Frequency Control*, Vol 35, No. 6, November 1988, pp. 711 - 717, and "Metalorganic Deposition (MOD): A Nonvacuum, Spin-on, Liquid-Based, Thin Film Method", *Materials Research Society Bulletin*, October 1989, pp. 48-53. However, the quality of the thin films made in these references was far too poor for use in integrated circuits, and these processes have, up to the time of the present invention, been used only for screen printing of metal oxide inks in making relatively macroscopic parts of circuits. Thus this spin-on technique did not appear to be a suitable candidate for a fabrication process which might produce state-of-the-art integrated circuit devices, such as high-capacitance, high-frequency thin film capacitors. Since the use of the GaAs substrate technology and the carboxylate spin-on technology both lead to less satisfactory results than, say, the silicon-based technology and deposition by sputtering, it would seem unlikely that their combination could lead to metal oxide thin film capacitors having high capacitance at high frequencies, i.e., at frequencies of 1 gigahertz and higher.

3. Solution to the problem:

The invention solves the problem of providing high-capacitance, high-frequency thin film capacitors by utilizing alkoxycarboxylate liquid precursors and a spin-on technique to deposit the metal oxide thin films on gallium arsenide substrates. Preferably the gallium arsenide is encapsulated by a barrier layer which prevents the volatilization of the GaAs in subsequent annealing steps at high temperature, which is in turn covered by a stress-reducing layer which lowers the stress between the gallium arsenide and the metal oxide capacitor. Preferably the barrier layer is comprised of silicon nitride (Si_3N_4) and the stress-reduction layer is comprised of silicon dioxide. Preferably a relatively low temperature spin-on process as described in copending and co-owned United States patent application Serial No. 08/165,082, is used to deposit the metal oxide.

The use of a liquid precursor spin-on process to deposit the metal oxide permits much more accurate control of the stoichiometry of the metal oxide and also results in a much more homogeneous material. This homogeneity and careful control of the drying and annealing processes leads to electronic properties that are

much better than for thin film devices fabricated by prior art methods. Further, the homogeneity of the metal oxides significantly reduces the stresses and cracking that accompanied prior art fabrication methods. Numerous other features, objects and advantages of the invention will become apparent from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of an integrated circuit capacitor according to the invention;

FIG. 2 is a graph of capacitance in farads (F) versus frequency in gigahertz (GHz) for BST capacitors fabricated according to the process of the invention and annealed at three different temperatures; and

FIG. 3 is a flow chart of an exemplary process according to the invention for fabricating a thin-film capacitor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Turning to FIG. 1, a thin film capacitor 10 as fabricated in the examples discussed below is shown. The capacitor 10 is formed on a single crystal gallium arsenide (GaAs) wafer 11 encapsulated by a barrier layer 12, preferably of silicon nitride (Si_3N_4), and a stress-reduction layer 14, preferably of silicon dioxide. The capacitor 10 includes a first electrode 16 formed of an adhesion layer 18, preferably of titanium of about 200 Å thickness, and a layer 20, preferably of platinum of about 2000 Å thickness. Capacitor 10 also includes a layer 22 of a metal oxide, such as BST, then a second electrode layer 24, also preferably about 2000 Å thick and made of platinum.

In the integrated circuit art, the GaAs crystal 11 is often referred to as a "substrate". Herein, "substrate" may be used to refer to the GaAs layer 11, but more generally will refer to any support for another layer. For example, the substrate 23 for the metal oxide layer 22 is, immediately, the platinum first electrode layer 20, but also can be interpreted broadly to include the layers 18, 14, 12 and 11 as well. The term "metal oxide" herein means a material of the general form ABO_3 where A and B are cations and O is the anion oxygen. The term is intended to include materials where A and B represent multiple elements; for example, it includes materials of the form $A'A''BO_3$, $AB'B''O_3$, and $A'A''B'B''O_3$, where A', A'', B' and B'' are

different metal elements. Preferably, A, A', A", are metals selected from the group of metals consisting of Ba, Bi, Sr, Pb, Ca, and La, and B, B', and B" are metals selected from the group consisting of Ti, Zr, Ta, Mo, W, and Nb. Preferably the metal oxide is a perovskite. Many of these metal oxides are ferroelectrics, though some that are classed as ferroelectrics may not exhibit ferroelectricity at room temperature. However, since most such ferroelectrics have relatively high dielectric constants, these materials are often useful in high dielectric constant capacitors, whether or not they are ferroelectric. Preferably, the metal oxide is barium strontium titanate (BST) and preferably has the formula $Ba_{0.7}Sr_{0.3}TiO$. The BST may be doped as described in copending United States patent application Serial No. 08/273,592.

Many other materials may be used for any of the layers discussed above, such as layer 18 may comprise tantalum, nickel, tantalum silicide, titanium silicide, nickel silicide, palladium and other materials as well as titanium and layer 20 may be other materials as well as platinum. The electrode 16 may also be formed of more than two layers and the electrode 24 may be formed of more than one layer. Further, it should be understood that FIG. 1 is not meant to be an actual cross-sectional view of any particular portion of an actual electronic device, but is merely an idealized representation which is employed to more clearly and fully depict the structure and process of the invention than would otherwise be possible. For example, the relative thicknesses of the individual layers are not shown proportionately, since otherwise, some layers, such as the substrate 11 would be so thick as to make the drawing unwieldy. It should also be understood that the capacitor 10 preferably forms a portion of an integrated circuit 30 which includes other electronic devices, such as transistors, other capacitors etc., which other devices are not shown for clarity. In addition, the metal oxide layer 22 may be incorporated into other devices, such as ferroelectric FETs, as well as capacitors.

Turning now to FIG. 3, a flow chart of the process for fabricating capacitors 10 according to the invention is shown. The process shall be discussed in terms of the embodiment of FIG. 1, but could just as well be discussed in terms of the other embodiments also. In step 41 a GaAs substrate 11 is provided. This substrate 11 is made according to conventional methods of growing GaAs crystals. In step 42 a layer of silicon nitride of about 1500 Å thick is deposited, preferably by plasma

enhanced chemical vapor deposition (PECVD), although other methods may also be used. Then a layer 14 of silicon dioxide about 1000 Å thick is deposited in step 43, by any conventional method, such as PECVD or wet growth. In step 44 a first electrode 16 is deposited. Preferably first electrode 16 comprises an adhesion layer 18, preferably of titanium and about 200 Å thick, and a layer 20 of platinum about 2000 Å thick, both deposited preferably by sputtering. A metal oxide precursor is prepared in step 45; this may be just prior to the application step 47, but usually a stock solution is prepared and stored well prior to the application. The metal oxide is preferably barium strontium titanate, and the precursor is prepared as described in United States patent application Serial No. 08/132,744. The foregoing patent application discloses a method of making a metal oxide which utilizes the combination of a metal alkoxycarboxylate, such as a barium alkoxycarboxylate, and a metal alkoxide, such as titanium isopropoxide. Specifically, a BST precursor is made by reacting barium with 2-methoxyethanol and 2-ethylhexanoic acid, adding strontium, allowing the mixture to cool, adding titanium isopropoxide and 2-methoxyethanol, and heating to obtain a final BST concentration of about 0.5 moles. As disclosed in United States Patent application Serial No. 08/132,744 and co-owned United States patent application Serial No. 08/165,082, which were incorporated by reference in the corresponding United States patent application to the present application, during the heating, the maximum temperature is 116 °C which ensures that all isopropanol and water will be boiled out. Thus, the precursor is essentially anhydrous. If a dopant is to be added, a dopant precursor solution is prepared and added to the precursor in step 45. Just prior to the application step, a solvent exchange step 46 is preferably performed. That is, a stock solution prepared as above is removed from storage, and the solvent that is convenient for manufacturing and/or which makes a precursor that stores well, such as xylene, is exchanged for a solvent that has a good viscosity for the application process, such n-butyl acetate for a spinning application process. The exchange is performed by adding the new solvent and distilling out the old. Preferably, for a spin-on process the concentration of the spin-on precursor solution is 0.29 - 0.31 moles, which is controlled at the solvent exchange step 46. In step 47 the precursor is applied to the substrate 23, preferably by spinning at 1500 RPM to 2000 RPM for

20 seconds to 60 seconds. However, other application methods may be used, for example, a misted deposition process as described in United States patent application Serial No. 07/993,380, which is hereby incorporated by reference. In steps 48 and 50, the precursor is treated to form the metal oxide dielectric material 22 on substrate 23. The treating is preferably by drying and annealing. The drying is preferably in air or dry nitrogen, and preferably at a relatively high temperature as compared to the prior art, i.e. at from 200 °C to 500 °C. Typically it is performed at 400 °C for 2 minutes in air. This high temperature drying step has been found to be essential to obtain predictable properties in BST. After drying, if the film 22 is not of the desired thickness, the application and drying steps 47 and 48 are repeated until the desired thickness is reached. Usually two to three repetitions of steps 47 and 48 are required to reach the thickness of about 2000 Å. When the desired thickness is obtained, the dried precursor is annealed in step 50 to form dielectric 22. The annealing is referred to as the first anneal to distinguish it from a later anneal. The anneal is preferably performed in oxygen at a temperature of from 600 °C to 850 °C for from 1 minute to 90 minutes. Typically, it is performed at 700 °C for 60 minutes in O_2 in a push/pull process including 10 minutes for the "push" into the furnace and 10 minutes for the "pull" out of the furnace. Careful control of this anneal temperature and time is also essential for predicable results. The resulting layer 22 is preferably about 2000 Å thick. In step 51 a second electrode 24 is deposited, preferably by sputtering, and preferably formed of about 2000 Å thick platinum. The device is then patterned in step 52, which may comprise only the patterning of the second electrode if any patterning was done after deposition of the first electrode. It is important that the device be patterned before the second anneal step 53 so that patterning stresses are removed by the anneal and any oxide defects created by the patterning are corrected. The second anneal 53 is preferably performed at the same temperature as the first anneal though variance within a small temperature range of 50 °C to 100 °C about the first anneal temperature is possible. The time for the second anneal is preferably less than for the first anneal, generally being about 30 minutes, though again a range of times from about 1 minute to 90 minutes is possible depending on the sample. Again, careful control of the anneal parameters is important to obtain predictable results.

In some instances it is desirable to skip the second anneal altogether. Finally, in step 54 the device is completed and evaluated.

Three samples of a BST capacitor 10 were made from a stock precursor solution having a stoichiometric content of barium, strontium and titanium as specified in the formula $Ba_{0.7}Sr_{0.3}TiO$. The process was as described above, except that for the first sample the first and second anneal steps were performed at 800 °C, in the second sample the first and second anneal steps were performed at 700 °C, and in the third sample the first and second anneal steps were performed at 650 °C. The electrical properties of the samples were evaluated with results as shown in FIG. 3, a graph of capacitance in farads versus frequency in gigahertz. To provide a basis of comparison, the dotted horizontal line shows the capacitance for an ideal material with dielectric constant, ϵ, of 300. The capacitance of the sample annealed at 800 °C drops off sharply as the frequency approaches 1 gigahertz. The capacitance of the sample annealed at 700 °C does not drop off until beyond 1 gigahertz, and the capacitance of the sample annealed at 650 °C continues flat out to nearly 10 gigahertz. However, the value of the capacitance drops by a factor of about 5 between the sample annealed at 800 °C and the sample annealed at 700 °C, and by another factor of a little over 10 between the sample annealed at 700 °C and the sample annealed at 650 °C. As indicated by the dotted line, for the sample annealed at 700 °C, the capacitance is still significantly higher than the capacitance, say for silicon dioxide, which has a dielectric constant of about 3.9, thus using the process of the invention, it is possible to fabricate a material that has a high capacitance well beyond 1 gigahertz.

There have been described novel structures and processes for fabricating integrated circuits having high-capacitance, high-frequency thin film capacitors. It should be understood that the particular embodiments shown in the drawings and described within this specification are for purposes of example and should not be construed to limit the invention. Further, it is evident that those skilled in the art may now make numerous uses and modifications of the specific embodiment described, without departing from the inventive concepts. For example, other capacitor structures than that shown in FIG. 1 may be used and the capacitors and process of making them may be combined with a wide variety of other structures and

processes. Equivalent materials, different material thicknesses, and other methods of depositing the substrate and electrode layers may be used. It is also evident that the process steps recited may in some instances be performed in a different order. Or equivalent structures and processes may be substituted for the various structures and processes described.

CLAIMS

We claim:

1. A method of fabricating a high capacitance thin film capacitor device, said method comprising the steps of: providing a gallium arsenide substrate (11); forming a barrier layer (12) on said substrate; forming a first electrode (16); forming a dielectric material (22) on said first electrode; and forming a second electrode (24) on said dielectric material, said method characterized in that said step of forming a dielectric material comprises:

providing a liquid precursor comprising a solution including barium, strontium, and titanium metal moieties in effective amounts for yielding a solid dielectric barium strontium titanate upon treating of said liquid precursor;

applying said liquid precursor to said first electrode (16); and

treating said liquid precursor on said first electrode to form said dielectric material comprising barium strontium titanate (22).

2. A method as in claim 1 characterized in that said step of providing a liquid precursor includes providing a solution comprising said barium, strontium, and titanium metal moieties in a first solvent, and then performing a solvent exchange step to provide said liquid precursor comprising a second solvent.

3. A method as in claim 1 characterized in that said liquid precursor comprises a metal alkoxycarboxylate.

4. A method as in claim 1 and further characterized in the step of forming a stress reduction layer (14) between said steps of forming a barrier layer (12) and forming a first electrode (16).

5. A method as in claim 4 characterized in that said stress reduction layer (14) comprises silicon dioxide of about 1000 Å thickness and said barrier layer (12) comprises Si_3N_4 of about 1500 Å thickness.

6. A method as in claim 1 characterized in that said step of treating comprises heating said precursor on said electrode (16) to a temperature of from 200 °C to 500 °C and said step of treating comprises annealing said precursor on said electrode at a temperature of between 600 °C and 850 °C.

7. A method as in claim 1 characterized in that said step of treating comprises a first anneal of said barium strontium titanate (22) for a time between

1 minute and 90 minutes and a second anneal of said barium strontium titanate for a time between 1 minute and 90 minutes.

8. A method as in claim 1 characterized in that said barium strontium titanate (22) has the formula $Ba_{0.7}Sr_{0.3}TiO_3$.

9. A method as in claim 1 characterized in that said step of forming a first electrode (16) comprises: forming an adhesion layer (18) selected from the group titanium, tantalum, nickel, tantalum silicide, nickel silicide, and palladium; and forming a second layer (20).

10. A high capacitance thin film capacitor device comprising: a gallium arsenide substrate (11); a barrier layer (12) formed on said substrate; a stress reduction layer (14) on said barrier layer; and a capacitor (10) on said stress reduction layer, said capacitor comprising a first electrode (16), a second electrode (24), and a dielectric material (22) between said electrodes, said method characterized in that said dielectric material comprises barium strontium titanate.

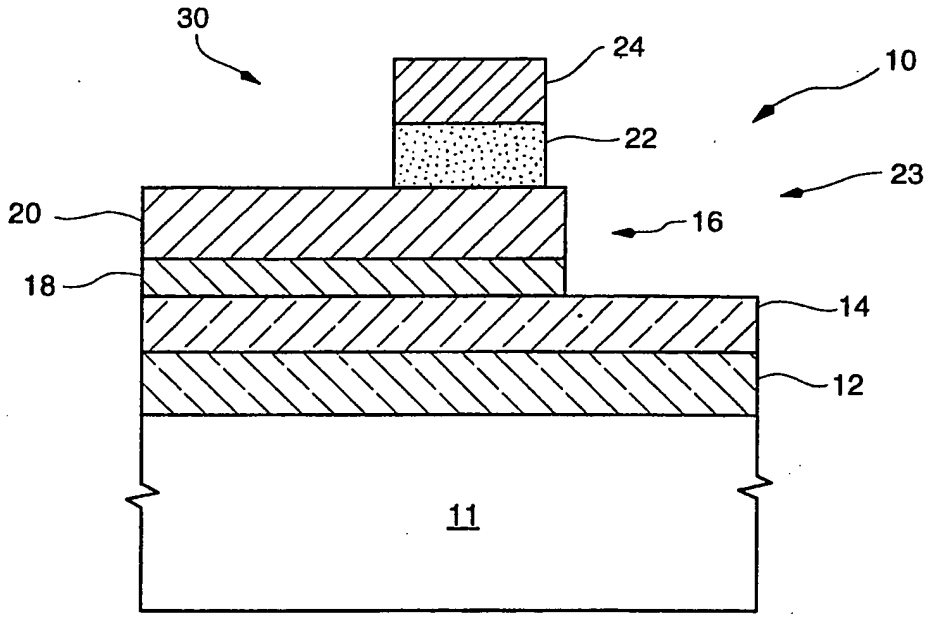
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FIG. 1

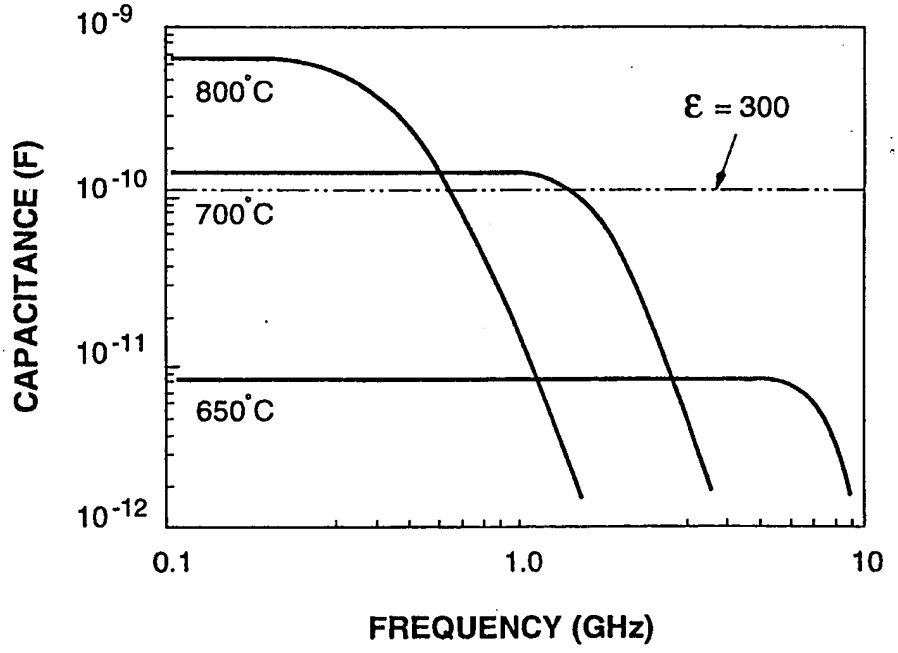
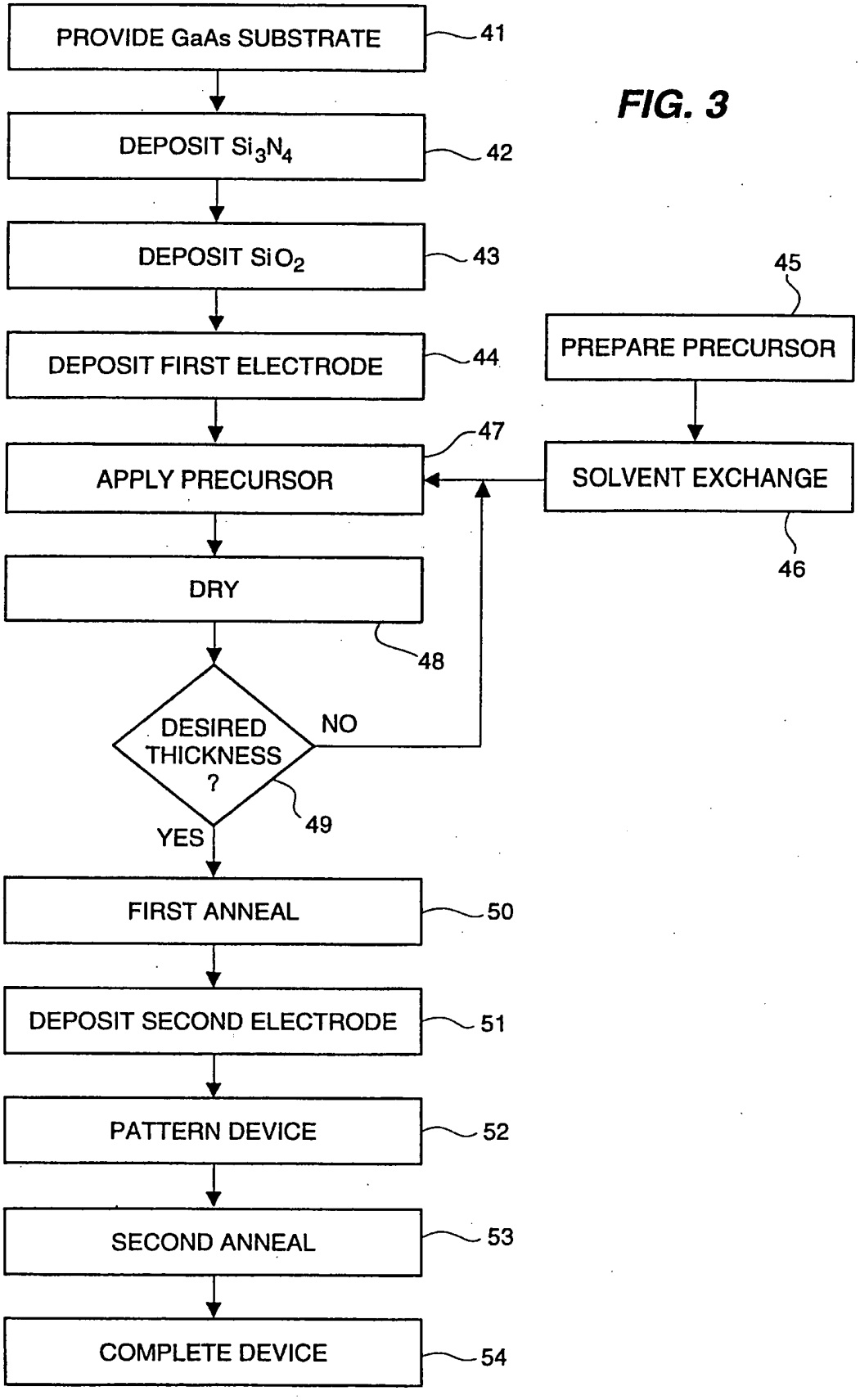

10^{-9}
10^{-10}
10^{-11}
10^{-12}
800°C
700°C
650°C
ε = 300
CAPACITANCE (F)
0.1
1.0
10
FREQUENCY (GHz)

FIG. 2


PROVIDE GaAs SUBSTRATE
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DEPOSIT Si_3N_4
42
DEPOSIT SiO_2
43
DEPOSIT FIRST ELECTRODE
44
APPLY PRECURSOR
47
DRY
48
DESIRED THICKNESS ?
49
NO
YES
FIRST ANNEAL
50
DEPOSIT SECOND ELECTRODE
51
PATTERN DEVICE
52
SECOND ANNEAL
53
COMPLETE DEVICE
54
45
PREPARE PRECURSOR
SOLVENT EXCHANGE
46

FIG. 3

INTERNATIONAL SEARCH REPORT

Interna' l Application No
PCT/US 95/03254

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/3205

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L H01G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JEE (JOURNAL OF ELECTRONIC ENGINEERING), JUNE 1993, JAPAN, vol. 30, no. 318, ISSN 0385-4507, pages 101-104, NOMA A 'Evolution of GaAs ICs containing ferroelectric capacitor' see page 101, column 2, paragraph 2 - page 103, column 1, paragraph 2 --- -/--	1,8-10

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

Interna l Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DEFECT PROPERTIES AND PROCESSING OF HIGH-TECHNOLOGY NONMETALLIC MATERIALS SYMPOSIUM, BOSTON, MA, USA, 2-4 DEC. 1985, ISBN 0-931837-25-1, 1986, PITTSBURGH, PA, USA, MATER. RES. SOC, USA, pages 35-42, VEST G M ET AL 'Synthesis of metallo-organic compounds for MOD powders and films' cited in the application see page 40, paragraph 2 - page 41, paragraph 3 ---	1,3
A	THIRD INTERNATIONAL SYMPOSIUM ON INTEGRATED FERROELECTRICS, COLORADO SPRINGS, CO, USA, 3-5 APRIL 1991, ISSN 1058-4587, INTEGRATED FERROELECTRICS, 1992, UK, pages 231-241, SANCHEZ L E ET AL 'Process technology developments for GaAs ferroelectric nonvolatile memory' cited in the application see page 235 - page 236 see figure 9 ---	1,4,5,10
A	WO,A,93 12542 (SYMETRIX CORP) 24 June 1993 cited in the application see page 23, line 9 - line 20 -----	2,3

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internat Application No
PCT/US 95/03254

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		AU-B-	3273893	19-07-93
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		EP-A-	0616723	28-09-94
		JP-T-	7502149	02-03-95
		JP-T-	7502150	02-03-95
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		US-A-	5316579	31-05-94
		US-A-	5423285	13-06-95
		CA-A-	2145878	11-05-94
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		WO-A-	9410702	11-05-94
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		WO-A-	9410084	11-05-94